PA - IDC

QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	10/008,683	Prepared by	Lois Stone	Tracking Number	5899170
Examiner-GAU	Norton - 1765	Date	3/18/04	Week Date	6/2/04
		No. of queries	1	IFW	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

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f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

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MESSAGE

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Copy provided for reference. Please advise.

Paul Pysher 617-542-5070 (MA)
10559/584001/P12765
fax 617-542-8906

called 3/25, faxed pg, he's getting appl'n file from CA

Thank you,

initials LL

RESPONSE Attorney faxed complete page. Data now present.

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E-5 (Rev. 10/01/02)

width W_1 suitable for a transistor channel length, e.g., of 0.03 micrometers (μm).

Referring to Fig. 3, portions of polysilicon layer 14 and gate oxide layer 12 are etched by, e.g., dry etching in a high density plasma etching system such as the Silicon Etch DPS II Centura™ 300 system, manufactured by Applied Materials, Inc., Santa Clara, California. Portions of polysilicon layer 14 and gate oxide layer 12 not in a shadow of photoresist masking feature 16, i.e. not underneath feature 16, are removed during etching. The etching thereby forms a polysilicon gate electrode 18.

Referring to Fig. 4, photoresist masking feature 16 is stripped off, leaving polysilicon gate electrode 18 and gate oxide 12 on silicon substrate 10.

Referring to Fig. 5, a first ion implantation is made into silicon substrate 10 to form a lightly doped source region 20 and a lightly doped drain region 22. For a p-channel device, a p-type dopant, such as boron, may be implanted into lightly doped source 20 and lightly doped drain 22 regions.

Referring to Fig. 6, a first sidewall spacer 24 and a second sidewall spacer 26 are formed proximate a first side 28 and a second side 30 of polysilicon gate electrode 18, respectively. First and second sidewall spacers 24, 26 are